A HETEROSTRUCTURE FET WITH 75.8-PERCENT POWER ADDED EFFICIENCY AT 10 GHz

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ABSTRACT

We are reporting the performance of a new AlGaAs/GaAs heterostructure FET (HFET), designed to have very high efficiency at X-band with high drain bias (9 volts and above). The combination of low doped (high 10^{16} cm^{-3}) AlGaAs under the gate and highly doped (mid 10^{17} cm^{-3}) GaAs channel and superlattice buffer layer allow high gate-drain and source-drain breakdown voltage (more than 20 volts), constant transconductance and moderate to high maximum channel current (350 to 450 mA/mm). These characteristics make the devices ideal for Class B and Class F operation. The 1200 x 0.25-µm HFET devices have demonstrated a record power-added efficiency (PAE) of 75.8 percent with 603 mW of output power and 8.8 dB of gain with a 9-volt drain bias at 10 GHz. Other 1200 x 0.25-µm HFET devices have demonstrated 63.2-percent PAE with 8.3 dB of gain and 851 mW of output power with a 12-volt drain bias. At 14 volts, we have measured 50-percent PAE with 7.4-dB gain and 1.1 watts of output power.

INTRODUCTION

Two requirements critical to phased array radars are high-efficiency modules and high-operating voltages in order to minimize the power dissipated in both the microwave amplifier and in the power distribution network.

AlGaAs/InGaAs pseudomorphic HEMTs have demonstrated excellent performances both at X-band[1] and Ku-band[2] but the drain operating voltage for maximum performance is low due to gate-drain breakdown voltages of 12 to 16 volts[1] and 7.2 volts[2].

We have developed an HFET device with high source-drain breakdown voltages (defined as 1 mA/mm of drain-to-source leakage current with the device pinched off) of up to 24 to 26 volts and constant transconductance which makes the device suitable for Class B and Class F operation.

DEVICE STRUCTURE AND CHARACTERISTICS

The material structure for the high performance HFET is shown in Figure 1. It includes a thin GaAs layer doped low to mid 10^{17} cm^{-3} sandwiched between a superlattice buffer layer on the bottom and a low doped (mid to high 10^{16} cm^{-3}) AlGaAs layer. A n+ GaAs cap layer completes the structure. The device structure includes a 1.5-µm "wide recess" etched into the GaAs n+ layer and into the AlGaAs low doped layer and a conventional gate recess. Gate length is 0.25 µm. Typical I-V characteristics for the HFETare shown in Figure 2. Low output conductance and constant transconductance with gate voltage are observed. This is further illustrated in Figure 3, which shows transconductance (g_m) and drain current (I_d) as a function of gate voltage with the drain at 3 volts.

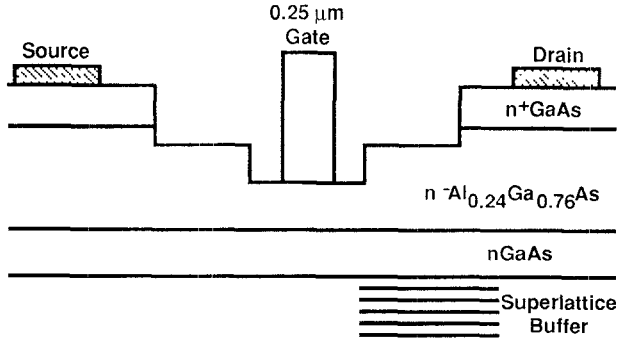

Figure 1. AlGaAs/GaAs Heterostructure FET

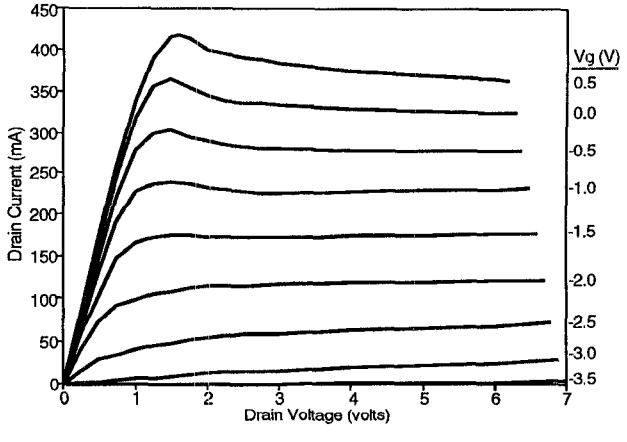

Figure 2. AlGaAs/GaAs HFET I-V Characteristics

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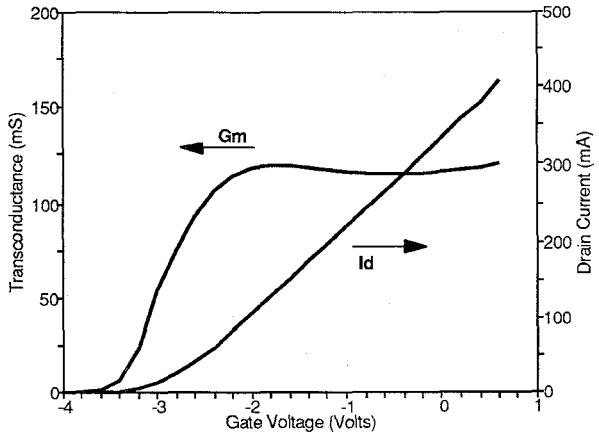

Figure 3. Transconductance and Drain Current as a Function of Gate Voltage

These characteristics of low output conductance and constant g_m are ideal for high efficiency operation. The small signal equivalent model for a typical 1200 x 0.25 µm HFET is shown in Figure 4, with the element values derived from best fit to measured S-parameters shown in Table 1.

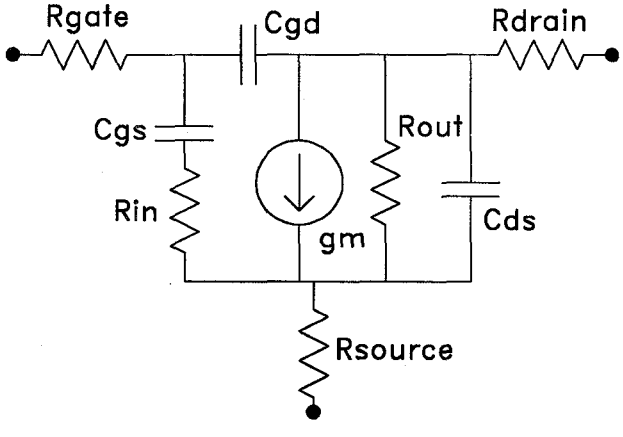

Figure 4. Small Signal Equivalent Model

RF RESULTS

A special fixture, shown in Figure 5, is used to characterize the devices for power, gain, and efficiency at 10 GHz. The devices are mounted on thin brass carriers which are sandwiched between input and output test blocks. The test blocks consist of prematched input and output circuits using 10-mil-thick alumina with 3.5-mm connectors for input/output connections. Tuning chips are placed along the matching circuits as needed to obtain optimum rf performance. Test blocks with prematched circuits have been designed for both 600- and 1200-µm FETs. The measured insertion loss for the 400-mil-long alumina network and connector is 0.2 dB at 10 GHz.

TABLE 1. 1200 x 0.25 µm HFET SMALL SIGNAL MODEL ELEMENTS VALUES

Element	R-5013#5
C_{gs}	0.95 pF
C_{gd}	0.072 pF
C_{ds}	0.34 pF
R_{gate}	1.0 Ω
R_{source}	1.3 Ω
R_{drain}	1.5 Ω
R_{in}	0.0 Ω
R_{out}	103 Ω
g_m	108 mS

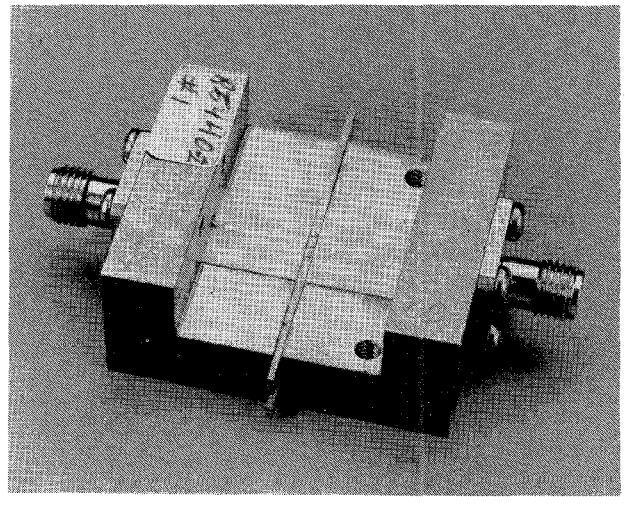

Figure 5. 10-GHz Test Fixture Showing Hard-Tuned Device

A number of devices have been "hard-tuned" for maximum efficiency at 10 GHz with gold ribbon straps welded in place of the chips. This allows the device to be tested as an amplifier multiple times on different test sets for measurement verification. Hard tuning also facilitates measurement of the optimum load required for maximum efficiency or power, depending on how the device was tuned. The load is measured by removing the output block (including the bondwire) and connecting it to a 50-Ω calibrated test block.

Figure 6 shows the power and efficiency for two "hard-tuned" 1200-µm HFETs over frequency with the input and output circuit losses de-embedded. The devices were tuned for maximum efficiency at 10 GHz and demonstrated 72- to

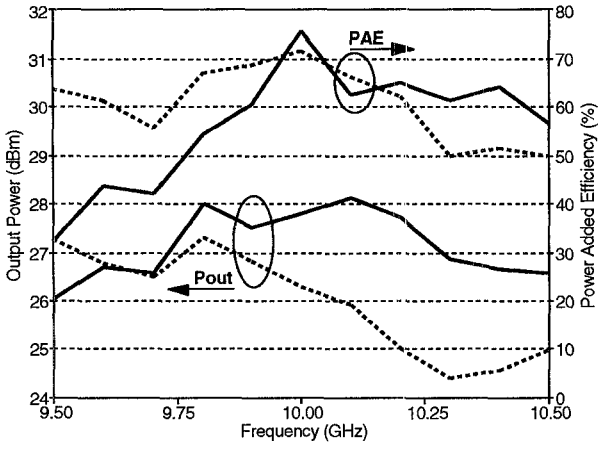

Figure 6. Power and PAE of R-5013 #5(——) and #2 (····) with Input Power of 19 dBm

75-percent peak power-added efficiencies at the 0.6-watt power level. Both of these devices were operated in a near class-B bias condition with Vd = 9 V. Figure 7 shows the output power, PAE, and Id as a function of input power for a 600-µm HFET from another wafer at 10.25 GHz. This device showed very good class B operating conditions with a quiescent bias current of just 70 µA at Vd = 9 V. As a result of the class B bias, the gain of the device under RF drive increased from 1.5 dB at low drive levels to a 9.5 dB maximum. Maximum efficiency occurred at about 1-dB gain compression. Table 2 summarizes the performance for these devices at 10 GHz.

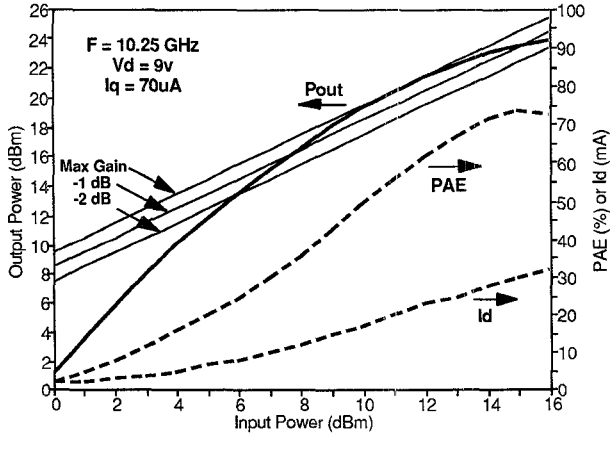

Figure 7. Output Power, PAE, and I_d of R-5440-2 #1 at 10.25 GHz

TABLE 2. 10-GHz HFET PERFORMANCE

Device Id	Power (mW)	Gain (dB)	PAE (%)
R-5013#5-1200 µm	603	8.8	75.8
R-5013#2-1200 µm	420	7.3	71.7
R-5440-2#1-600 µm	258	9.1	74.4

The output networks were removed and the optimum load impedance were measured for a number of 1200-µm HFETs. Figure 8 shows the IV curves for a typical 0.25 × 1200 µm HFET with two resistive load lines superimposed. The load line for maximum output power is displayed along with the measured load line resulting in maximum efficiency. It is evident that tuning for maximum efficiency occurs at the expense of maximum power. During the characterization procedure approximately 1.5 dB of output power was traded for 5 percentage points of improved efficiency. This was accomplished by reducing voltage swing losses in the linear region of the IV curves. LIBRA large signal analysis using the measured load impedance indicates that the effective V_{SAT} is around 0.4 volt for the maximum efficiency load line versus 1.5 volts for maximum power load line.

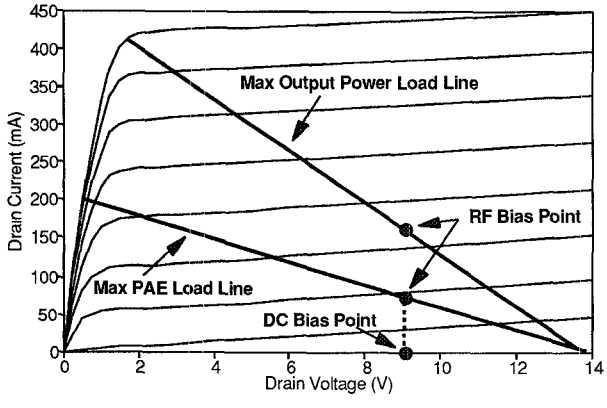

Figure 8. Maximum Power and PAE Load Lines for 1200 µm HFET

We are confident of our power and efficiency measurements due to verification of the measurements on several different calibrated test sets. The maximum PAE summarized in Table 2 is 75.8 percent (corresponding to a drain efficiency of 86.9 percent). For comparison, Snider[3] derives the maximum drain efficiency for an overdriven class B power amplifier to be 88.6 percent. His derivation assumes a 0 volt saturation voltage and a sinusoidal input signal. Additionally, Hall[4] indicates that harmonic tuning of the source improves the efficiency in Class C amplifiers. Measurements of our "hard-tuned" input circuits indicate the use of harmonic tuning for improved efficiency.

CONCLUSION

A new HFET using an AlGaAs/GaAs structure has demonstrated a record 75.8-percent power added efficiency at 10 GHz with 603 mW of output power and 8.8 dB of gain. The high breakdown voltage of the device combined with constant g_m result in optimum performance at Vd = 9 V and a Class B bias.

ACKNOWLEDGEMENTS

The authors gratefully acknowledge Faye Goodman for assembly of the fixtured devices and Bob Smith for many - many hours of tedious chip tuning of devices.

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